CLAIMS:

1. A system comprising:

a first ASIC (Application Specific Integrated Circuit) including a first substrate;

a plurality of On Chip Macros mounted on said first substrate;

a second ASIC including a second substrate positioned in spaced relationship to said first substrate;

a plurality of On Chip Macros mounted on said second substrate;

a Chip to Chip Bus Interface subsystem operatively positioned to provide communications between the first ASIC and the second ASIC; and

a Chip to Chip Macro subsystem operatively mounted on the first ASIC and the second ASIC, said Chip to Chip Macro subsystem aggregating all communications between at least a pair of On Chip Macros one of each being located on the first substrate and the second substrate onto the Chip to Chip Bus Interface subsystem.

2. The system of Claim 1 wherein the Chip to Chip bus interface subsystem includes a first transmission system transmitting data from the first ASIC to the second ASIC; and

a second transmission system transmitting data from the second ASIC to the first ASIC.

3. The system of Claim 2 wherein the first transmission system includes a first unidirectional data bus;

a first unidirectional parity bus;

a first unidirectional start of message control line; and

a first unidirectional clock bus.

4. The system of Claim 3 wherein the first transmission system further includes a first control line that transmits a signal in a direction opposite to signal transmission on other lines in said first transmission system, said signal inhibiting a Macro on a selected ASIC from transmitting data.

5. The system of Claim 2 wherein the second transmission system includes a set of transmission lines substantially similar to those set forth in Claim 4.

6. The system of Claim 5 further including a second control line that transmits signals in a direction opposite to signal transmission on other lines in said second transmission systems.

7. The system of Claim 1 wherein the Chip to Chip Macro subsystem includes a first Chip to Chip Macro operatively mounted on the first ASIC; and

a second Chip to Chip macro operatively mounted on the second ASIC.

8. The system of Claim 7 wherein the first Chip to Chip macro or the second Chip to Chip macro includes a transmit (Tx) channel; and

a Receive Channel wherein said Tx channel includes a transmitter Multiplexor;

a transmitter Speed Matching Buffer connected in series to the transmitter Multiplexor; and

a Serializer connected in series to the transmitter speed matching buffer; and said Receive Channel includes a De-serializer; Receive (Rx) Speed Matching buffer connected in series to the De-Serializer and a Rx De-multiplexor connected in series to the Rx Speed Matching buffer.

9. The system of Claim 8 wherein the Tx Multiplexor further includes arbitration devices receiving requests from multiple Macros and granting priority to transmit to one of said requests; and

a generator response to the one of said requests to generate a message based upon information in the one of said requests and forward said message to the speed matching buffer.

10. The system of Claim 8 wherein the Rx De-mulitplexor includes a decoder that decodes selected fields in messages to determine which Macro should receive the message.

11. A Macro for interconnecting chips comprising:

a Transmit channel; and

a Receive channel; said Transmit Channel including an arbitrator that arbitrates Requests generated from multiple Requesters and granting priority to one of the requests;

a generator responsive to said one of the requests to generate a message based upon information in said one of the requests;

a first Speed Matching Buffer that receives the message; and

a Serializer extracting messages from said Speed Matching Buffer at a first data rate over a relatively wide data bus and converting said message to a second data rate for transmission over a data bus narrower than the relatively wide data bus.

12. The Macro of Claim 11 wherein the Speed Matching Buffer includes a RAM; and

a controller coupled to said RAM, said controller causing data to be written in said RAM at a first frequency and read from said RAM at a different frequency.

13. The Macro of Claim 11 wherein the Receive Channel further includes

a second Speed Matching Buffer that buffers messages received from another macro;

a De-serializer receiving the messages having a first footprint and first data rate from another macro, said De-serializer adjusting the first footprint and first data rate of the messages from another macro and loading said messages into the second Speed Matching Buffer; and

a De-Multiplexor including circuits to extract messages from the Speed Matching Buffer, determining destination of extracted messages and forwarding the extracted message to determined destinations.

14. The Macro of Claim 12 further including circuit in said second Speed Matching Buffer to generate a control signal if said second speed matching buffer does not wish to receive additional data.

15. The Macro of Claim 11 or Claim 13 further including a Network Processor Complex Chip operatively coupled to said Macro.

16. The Macro of Claim 11 or Claim 13 further including a Scheduler Chip operatively coupled to said Macro.

17. The Macro of Claim 11 or Claim 13 further including a Data Flow Chip operatively coupled to the Macro.

18. A method comprising:

partitioning circuits into functional blocks on a first ASIC and a second ASIC;

generating Request signals by functional blocks on the first ASIC wanting to communicate with functional blocks on the second ASIC;

granting priority to one Request based upon a result of an arbitrator arbitrating between multiple Requests;

generating a message based upon information in the one Request;

buffering the message in a first buffer; and

serializing buffered messages with a Serializer to permit data transmitted at a first data rate on a wide internal ASIC bus to be transferred on a narrower bus at a higher data rate.

19. The method of Claim 18 wherein the internal ASIC bus is approximately 128 bits.

20. The method of Claim 19 wherein the narrower bus is approximately 32 bits and the higher data rate is approximately 500Mbit/sec (per bit).

21. The method of Claim 18 further including the steps of providing on the first ASIC a second buffer to receive messages from the second ASIC;

converting the message by a De-serializer from a first footprint, equivalent to a width of a first bus, and first data rate to a second footprint, equivalent to a width of a second bus, and second data rate; and

writing converted messages into the second buffer.

22. The method of Claim 21 further including the steps of extracting by a De-multiplexor messages from said second buffer;

determining by said De-multiplexor a destination for said extracted messages; and

forwarding said extracted messages to the destination.

23. The system of Claim 1 wherein the first ASIC includes a Network Processor Complex Chip and the second ASIC includes a Data Flow Chip.

24. The system of Claim 1 where the first ASIC includes a Data Flow Chip and the second ASIC includes a Scheduler chip.

25. A system comprising:

a Data Flow Chip;

a first Chip to Chip Macro operatively mounted on said Data Flow Chip;

a Schedule Chip;

a second Chip to Chip Macro operatively mounted on said Data Flow Chip;

a transmission interface interconnecting the first Chip to Chip Macro and second Chip to Chip Macro.

26. A device comprising:

an ASIC having circuits that can be grouped into separate sub Macros; and

a Chip to Chip Macro mounted on said ASIC, said Chip to Chip macro receiving data at a first data rate with a first footprint from selected ones of said sub Macros converting the data to a second footprint at a second data rate and transmitting the data at the second data rate and second footprint.

27. The device of Claim 26 wherein the second footprint is narrower than the first footprint and the second data rate is higher than the first data rate.